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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOEL HOWARD SCHOPP

Appeal 2008-006153
Application 10/677,661[1]
Technology Center 2100

Decided: November 12, 2009

Before LEE E. BARRETT, JAY P. LUCAS, and STEPHEN C. SIU, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals from a final rejection of claims 1, 3, 4, 6-10, 12, 13, 15-17 and 19-28 under authority of 35 U.S.C. § 134(a). Claims 2, 5, 14 and

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[1] Application filed October 2, 2003. The real party in interest is International Business Machines Corporation.

18 are cancelled. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellant's invention relates to a method for optimizing caching within a logical partitioned data processing system. In the words of Appellant:

> The present invention provides a method, apparatus, and computer instructions for assigning processors to partitions in a multi-processor data processing system. Optimal allocation sets are generated for unallocated processors in the multi-processor data processing system for a cache level. Each set includes an allocation of unallocated processors to at least one partition. A determination is made as whether a set in the optimal allocation sets match requirements for a set of partitions selected for the data processing system. In response to a match existing, processors in the set are removed from the unallocated processors, wherein cache usage by the processors is optimized for the cache level.

(Spec. 4).

Claim 1 and claim 17 are exemplary:

1. A method for assigning processors to partitions in a multi-processor data processing system, the method comprising:

generating optimal allocation sets for unallocated processors in the multi-processor data processing system for a cache level, wherein each optimal allocation set includes an allocation of unallocated processors to at least one partition;

determining whether a first set in the optimal allocation sets matches requirements for a set of partitions selected for the data processing system; and

responsive to a match existing, removing processors in the first set from the unallocated processors to form a group of removed processors, wherein cache usage by the group of removed processors is optimized for the cache level.

17. A computer program product in a computer recordable-type medium for assigning processors to partitions in a multi-processor data processing system, the computer program product comprising:

first instructions for generating optimal allocation sets for unallocated processors in the multi-processor data processing system for a cache level, wherein each optimal allocation set includes an allocation of unallocated processors to at least one partition;

second instructions for determining whether a first set in the optimal allocation sets matches requirements for a set of partitions selected for the data processing system;

third instructions for, responsive to a match existing, removing processors in the first set from the unallocated processors to form a group of removed processors, wherein cache usage by the group of removed processors is optimized for the cache level.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Greenstein	US 5,784,702	Jul. 21, 1998
Arimilli	US 6,212,605 B1	Apr. 03, 2001
Olarig	US 2003/0065886 A1	Apr. 03, 2003 (filed on Sep. 29, 2001)
Mock	US 2003/0084372 A1	May 01, 2003
Arimilli	US 6,581,115 B1	Jun. 17, 2003

REJECTIONS

The Examiner rejects the claims as follows:

R1: Claims 1, 4, 8, 10 and 13 stand rejected under 35 U.S.C. § 102(e) for being anticipated by Olarig.

R2: Claims 3 and 12 stand rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Arimilli '605.

R3: Claims 6, 7, 15, and 16 stand rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Arimilli '115.

R4: Claims 9, 17, and 20 stand rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Mock.

R5: Claim 19 stands rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Mock and further in view of Arimilli '605.

R6: Claims 21 to 23 stand rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Mock and further in view of Arimilli '115.

R7: Claims 24, 25, 27 stand rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Greenstein.

R8: Claims 26, and 28 stand rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Mock and further in view of Greenstein.

Groups of Claims:

The claims will be discussed in the order of the rejections. *See* 37 C.F.R. § 41.37 (c) (vii). *See also In re McDaniel*, 293 F.3d 1379, 1383 (Fed. Cir. 2002) ("If the brief fails to meet either requirement [of 37 C.F.R. § 1.192(c)(7)], the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of

all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim.").

Appellant contends that the claimed subject matter is not anticipated by Olarig nor rendered obvious by Olarig in combination with the other references for failure of the references to teach the claimed limitations and to be properly combined. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Brief and the Answer for their respective details. Only those arguments actually made by Appellant have been considered in this opinion. Arguments that Appellant could have made but chose not to make in the Brief have not been considered and are deemed to be waived.

We affirm the rejections.

ISSUE

The issue is whether Appellant has shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a). The issue turns on whether Olarig teaches the unallocated processors and other limitations as claimed and whether there is a legally sufficient justification for combining the disclosures of Olarig and the other references.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellant has invented a method of assigning processors in a multiprocessor computer system to various partitions of the system; each

partition capable of processing a different program and requiring a different amount of resources, including cache, for its optimal performance (Spec. 3, Spec. 17). The invention searches at each level of cache and, in a number of passes, assigns optimal placements for processors into the various partitions. When optimal solutions are found, the previously unallocated processors and partitions are assigned to each other (Spec. 18, top). The process continues until all of the levels of cache are assigned their partitions and processors *(Id.)*.

2. Olarig teaches the allocation of cache into partitions to service a plurality of entities, such as processors or PCI ports. (Fig 1, # 120, 126 and 140). Each cache partition (cache bin) can be assigned to a different logical or physical entity. (¶ [0019]). The cache partitioning is tentatively optimized on start up but is repartitioned dynamically in operation to further optimize the partition resources for the load. (¶ [0011]).

3. Arimilli '605 is a patent for controlling the computer process called eviction of data from a cache. Data is evicted from a cache when it is no longer needed. Arimilli teaches a method of reserving certain flagged cache memories from eviction by setting a flag. (Col. 2, l. 58). The process is propagated through all the cache on a level by level basis, L1, L2, etc. (Col. 3, l. 55).

4. Arimilli '115 teaches, among other things, connecting processor chips of symmetric multiprocessor design (SMP) to multilevel cache memories, specifically level 1, level 2, and level 3 cache. (Col 5, l. 48; col. 6. l. 22).

5. Mock teaches a multiprocessor computer system with cache memory management at multiple levels, L1 and L2, on separate chips. (¶ [0034]).

6. Greenstein teaches a multiprocessor computer system with multiple partitions (LPAR) and dynamic resource configuration of the systems. (Col. 3, ll. 55-65).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313.

ANALYSIS

From our review of the administrative record, we find that the Examiner has presented arguments for the rejections of Appellant's claims under 35 U.S.C. §§ 102 and 103 on pages 3 to 13 of the Examiner's Answer. In opposition, Appellant presents a number of arguments.

Arguments with respect to the rejection of claims 1, 4, 8, 10 13 under 35 U.S.C. § 102(e) [R1]

The Examiner has rejected the noted claims for being anticipated by Olarig. Appellant argues "Olarig does not necessarily teach 'wherein each optimal allocation set includes an allocation of unallocated processors to at least one partition,' as claimed". (Br. 15, middle). Appellant states that "Olarig does not actually create an allocation of unallocated processors - the examiner simply assumes the existence of unallocated processors." (*Id.*).

The Examiner points to ¶ [0019] of the Olarig Patent Application Publication, "cache memory is partitioned, and dedicated to a different processor." (Ans. 14, middle). Appellant states that this is not an allocation of unallocated processors, but his argument is not based on any statements in the references. (Br. 15, middle). In the noted ¶ [0019] of the reference, we appreciate "cache 120 can be partitioned into two cache bins with one cache bin dedicated to the processor bus 160 and the other cache bin dedicated to the processor bus 162." There is no teaching, as proposed by the Appellant, that these processors attached to the bus were previously allocated. (*See* Fig. 1.) Thus, we are not persuaded that the rejection was in error on this point.

Appellant argues that there is no teaching in Olarig of generating optimal allocation sets, as claimed. In the noted ¶ [0019], Olarig teaches alternative partitions in order to optimize the resources. See Answer 18, middle, for the Examiner's rationale, which we endorse and adopt. After making the first presumptive allocation, Olarig teaches "a partitioned cache can be further optimized by reallocating the sizes of cache partitions." ([0021]).

Appellant further argues that Olarig does not teach the removing of the processors as claimed. The "dedication" or "allocation" of the selected processors in Olarig to a partition of the cache at a cache level, we find, anticipates the removing step, as noted by the Examiner in the Answer, page 19, middle.

Appellant has argued that the Examiner's interpretation of assigning sets of unallocated processors to partitions of the cache is unreasonable, relying on detailed analysis of the specification's description. (Br. 18-21). We find that the extra details of the specification are not reflected in the plain meaning of the claim language and that the Examiner's interpretation of the claim language is not unreasonable.

We do not find error with the rejection in this regard.

Arguments with respect to the rejection of claims 3 and 12 under 35 U.S.C. § 102 [R2]

The Examiner has rejected these claims over Olarig in view of Arimilli '605. Appellant argues that the combination of references does not

teach assigning processors to partitions as claimed in these claims. (Br. 26, middle). We find the contrary, as expressed in the analysis of [R1] above.

Appellant further argues the propriety of the combination of references, alleging that the references are addressed to different problems. (Br. 27, top). In the landmark case, *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 402 (2007), the Supreme Court commented that "It is common sense that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle." Appellant has repeated this argument concerning the propriety of combining references that address different problems in his discussion for each rejection. In view of this Supreme Court guidance, we conclude such arguments do not carry weight and are deemed unpersuasive in each instance, [R2] through [R8].

Appellant also argues that Arimilli '605 is non-analogous art. (Br. 28, middle). We fail to agree with the Appellant, for the reasons stated by the Examiner (Ans. 26, middle).

We do not find error with this rejection.

Arguments with respect to the rejection of claims 6, 7, 15, and 16 under 35 U.S.C. § 103 [R3]

The Examiner has rejected these claims over Olarig in view of Arimilli '115. Appellant argues that the combination of references does not teach assigning processors to partitions as claimed in these claims. (Br. 30, middle). We find the contrary, as expressed in the analysis of [R1] above.

Appellant's arguments concerning motivation to combine are similar to those expressed above for rejection [R2] and are not deemed persuasive. See the Examiner's Answer, page 28, bottom concerning analogous art.

Arguments with respect to the rejection of claims 9, 17 and 20 under 35 U.S.C. § 103 [R4]

The Examiner has rejected these claims over Olarig in view of Mock. Appellant argues that the combination of references does not teach assigning processors to partitions as claimed in these claims. (Br. 35, middle). We find the contrary, as expressed in the analysis of [R1] above.

Appellant further argues that Mock does not address the limitations of claim 9. Mock is cited for its teaching of the memory for storing instructions, clearly shown on the face of the Patent Application Publication and described in ¶ [0034]. The combination of Olarig and Mock, we find, is suitable for the Examiner's rejection under 35 U.S.C. § 103.

Appellant's arguments concerning motivation to combine are similar to those expressed above for rejection [R3] and are not deemed persuasive. See the Examiner's Answer, page 31, bottom concerning analogous art.

Arguments with respect to the rejection of claim 19 under 35 U.S.C. § 103 [R5]

The Examiner has rejected claim 19 over Olarig in view of Mock and Arimilli '605. Appellant argues that the combination of references does not

teach assigning processors to partitions as claimed in these claims. (Br. 38, bottom). We find the contrary, as expressed in the analysis of [R1] above.

Appellant's arguments concerning motivation to combine are similar to those expressed above for rejection [R4] and are not deemed persuasive. See the Examiner's Answer, page 34, top concerning analogous art.

Arguments with respect to the rejection of claims 21 to 23 under 35 U.S.C. § 103 [R6]

The Examiner has rejected claims 21-23 over Olarig in view of Mock and Arimilli '115. Appellant argues that the combination of references does not teach assigning processors to partitions as claimed in these claims. (Br. 41, bottom). We find the contrary, as expressed in the analysis of [R1] above.

Appellant's arguments concerning motivation to combine are similar to those expressed above for rejection [R5] and are not deemed persuasive. See the Examiner's Answer, page 36, top and the Findings of Fact section above concerning analogous art.

Arguments with respect to the rejection of claims 24 to 25, and 27 under 35 U.S.C. § 103 [R7]

The Examiner has rejected claims 24, 25, and 27 over Olarig in view of Greenstein. Appellant argues that the combination of references does not teach assigning processors to partitions as claimed in these claims. (Br. 44, bottom). We find the contrary, as expressed in the analysis of [R1] above.

Appellant's arguments concerning motivation to combine are similar to those expressed above for rejection [R6] and are not deemed persuasive. See the Examiner's Answer, page 38 to 39, and the Findings of Fact section above concerning analogous art.

Arguments with respect to the rejection of claims 26 and 28 under 35 U.S.C. § 103 [R8]

The Examiner has rejected claims 26 and 28 over Olarig in view of Mock and Greenstein. Appellant argues that the combination of references does not teach assigning processors to partitions as claimed in these claims. (Br. 48, bottom). We find the contrary, as expressed in the analysis of R1 above.

Appellant's arguments concerning motivation to combine are similar to those expressed above for rejection [R6] and are not deemed persuasive. See the Examiner's Answer, page 40 to 41, and the Findings of Fact section above concerning analogous art.

CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1, 3, 4, 6-10, 12, 13, 15-17 and 19-28 under the respective rejections [R1] to [R8].

DECISION

The Examiner's rejections [R1] to [R8] respectively of claims 1, 3, 4, 6-10, 12, 13, 15-17 and 19-28 are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

peb

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